



Course Name: Master of Technology (M. Tech.) in VLSI Design  
**Course Structure**

**FIRST YEAR**

<b>SEMESTER I</b>								
<b>Sl. No</b>	<b>Type</b>	<b>Course code</b>	<b>Course Title</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>Contact Hrs/wk</b>	<b>Credits</b>
1	Theory	EEC61131	Core-I: Advances in VLSI Design	3	0	0	3	3
2	Theory	EEC61133	Core-II: VLSI for Digital Signal Processing	3	0	0	3	3
3	Theory		Elective I	3	0	0	3	3
4	Theory		Elective II	3	0	0	3	3
5	Theory		Elective III	3	0	0	3	3
6	Practical	EEC61231	Core I Lab: VHDL Programming Laboratory	0	0	3	3	2
7	Practical	EEC61233	Core II Lab: VLSI for Digital Signal Processing Laboratory	0	0	3	3	2
8	Seminar	EEC61301	Seminar and Technical Writing-I	0	0	2	2	2
<b>Total</b>				<b>15</b>	<b>0</b>	<b>8</b>	<b>23</b>	<b>21</b>

<b>SEMESTER II</b>								
<b>Sl. No</b>	<b>Type</b>	<b>Course code</b>	<b>Course Title</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>Contact Hrs/wk</b>	<b>Credits</b>
1	Theory	EEC61132	Core III: Electronic Design Automation Tools	3	0	0	3	3
2	Theory	EEC61134	Core IV: Low Power VLSI System Design	3	0	0	3	3
3	Theory		Elective IV	3	0	0	3	3
4	Theory		Elective V	3	0	0	3	3
5	Theory		Elective VI	3	0	0	3	3
6	Practical	EEC61234	Core III Lab: ASIC - CAD Laboratory	0	0	3	3	2

7	Seminar	EEC61302	Seminar and Technical Writing-II	0	0	2	2	2
<b>Total</b>				<b>15</b>	<b>0</b>	<b>5</b>	<b>20</b>	<b>19</b>

**Total Credit (First Year): 40**

## SECOND YEAR

<b>SEMESTER III</b>								
Sl. No	Type	Course code	Course Title	L	T	P	Contact Hrs/wk	Credits
1	Dissertation	EEC62401	Thesis Part I	0	0	24	24	16
2	Seminar	EEC62301	Seminar and Technical Writing III	0	0	2	2	2
<b>Total</b>				<b>0</b>	<b>0</b>	<b>26</b>	<b>26</b>	<b>18</b>

<b>SEMESTER IV</b>								
Sl. No	Type	Course code	Course Title	L	T	P	Contact Hrs/wk	Credits
1	Dissertation	EEC62402	Thesis Part II	0	0	24	24	16
2	Seminar	EEC62302	Seminar and Technical Writing IV	0	0	2	2	2
3	Sessional	EEC62502	Grand Viva					4
<b>Total</b>				<b>0</b>	<b>0</b>	<b>26</b>	<b>26</b>	<b>22</b>

**Specializations: VLSI Design**

<b>EEC61135</b>	Secured Digital System Design
<b>EEC61137</b>	Modelling and Synthesis with Verilog HDL
<b>EEC61139</b>	Internet of Things
<b>EEC61123</b>	Bio Medical System Engineering
<b>EEC61125</b>	CMOS Analog VLSI Design
<b>EEC61126</b>	Visual Sensors and interfaces
<b>EEC61116</b>	VLSI Signal Processing
<b>EEC61151</b>	Fiber Optic Sensors
<b>ECS61153</b>	Artificial Intelligence
<b>EEC61132</b>	Analog and Digital CMOS VLSI Design
<b>EEC61134</b>	Embedded System Design
<b>EEC61136</b>	High Speed System Design
<b>EEC61138</b>	Mixed-Signal Circuit Design
<b>EEC61140</b>	Functional Verification using Hardware Description Languages
<b>EEC61142</b>	Image and Video Processing
<b>EEC61144</b>	Advanced Semiconductor Device Modelling
<b>EEC61146</b>	RF IC design
<b>ECS61148</b>	Soft Computing